# Optimizing Operating Temperature for CH7009/7010 DVI/TV Output Device

## Introduction

This application note focuses on how to optimize the operating temperature of the CH7009/7010 DVI/TV Output Device. Abnormal operating temperatures may cause the TV or DVI panel to display improperly. Furthermore, it may damage the device and render it inoperable.

CH7009/7010 may overheat if both TV and DVI outputs are turned on simultaneously. The CH7009/7010 device is not designed for supporting the simultaneous display of TV and DVI outputs. Therefore, the DACs and the DVI circuitry should not be turned on simultaneously. Software graphics driver should be carefully planned when programming the CH7009/7010 register settings. The Power Management Register (Reg. 49h) is the one that developers should pay close attention to.

### Power Management Register Setting

The Power Management Register controls which operating circuitry within the CH7009/7010 is used.

Power Management Register
Symbol: PM
Address: 49h
Bits: 8

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | DVIP | DVIL | TV | DACPD3 | DACPD2 | DACPD1 | DACPD0 | FPD |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | | | | 1 | 1 | 0 | 0 | 0 |

*The table shown below gives the suggested register settings*:

| DVIP | DVIL | TV | DACPD [3:0] | FPD | Operating State | Functional Description |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1001 | 0 | Composite Off, S-Video On | Composite DACs are off. |
| 0 | 0 | 1 | 0111 or 1110 | 0 | Composite On, S-Video Off | S-Video DACs are off. Either pin 39 CVBS/B or pin 36 CVBS can be used for composite out. |
| 0 | 0 | 1 | 0000 | 0 | All DACs On | Composite and S-Video are on. |
| 0 | 0 | 0 | 1111 | 0 | VGA to TV Encoder Off | TV off. |
| 1 | 1 | 0 | 1111 | 0 | DVI Encode, Serialize, transmitter, and PLL on. | DVI is in normal function. |
| X | X | X | XXXX | 1 | Full Power Down | All circuitry are powered down except serial port |

Remember to turn both DVIP and DVIL bits to “0” when TV is “1”, and vice-versa. This will help reduce the overall power consumption as well as the risk of over-stressing the encoder with unnecessary rising temperature. The only “don’t-care” condition permitted here is when the Full Power Down (FPD) bit is used.